

FORMING GATE OXIDES HAVING MULTIPLE THICKNESSES

TECHNICAL FIELD OF THE INVENTION

[0001] The invention relates to fabrication of gate oxides on semiconductor substrates and, more particularly, to the fabrication of multiple gate oxides having different thicknesses than one another.

BACKGROUND OF THE INVENTION

[0002] The scaling of gate dielectrics - also referred to as gate oxides - to smaller thickness is one of the key elements that enables the continued scaling of silicon complementary-metal-on-silicon (CMOS) technology to higher performance levels. Also, having multiple thicknesses for gate oxides (also called gate dielectrics) on a single integrated circuit (IC) chip is desirable to address power and performance concerns as well as input/output (I/O) circuit needs. The thin gate dielectrics are used for the high performance parts of the circuit design, however the thin gate dielectrics also have higher leakage, so they cannot be used on the entire chip. The thicker gate dielectrics are used for lower performance, non-critical devices, which reduces power dissipation by reducing gate leakage. Additionally, these thicker gate dielectric devices are needed to support I/O circuits that require high voltage operation. Thin gate dielectrics are generally unable to meet lifetime requirements at such high voltages.

[0003] Thinner gate dielectrics generate more inversion charge, and improve short-channel effects by increasing gate control of the channel. Because the gate dielectric is formed at the interface where the inversion layer is formed and transistor current is conducted, this bottom interface must be extremely high quality. As gate oxide thickness is

reduced below 20 Angstroms, even the top interface with the poly (polysilicon; poly-Si) has increasing influence on the conduction in the channel region, so is also important to maintain the quality of the gate oxide/poly-Si interface. The relative importance of this top interface becomes more and more significant as the gate oxide is reduced in thickness.

[0004] Typical physical thickness of advanced silicon oxynitride gate dielectric is only 13 Angstroms for 5-7 Si-O bonds. It is known that the top gate dielectric interface (the interface between a gate dielectric and a gate electrode) affect the overall electrical property of such thin dielectrics. For instance, an exposure of the oxynitride surface to water (H₂O) undesirably increases the dielectric thickness and replaces nitrogen atoms in the vicinity of the top interface with oxygen atoms undesirably reducing overall dielectric constant of the gate dielectric. In order to preserve such ultra thin gate dielectric, any exposure of gate dielectric to wet chemicals is avoided and the waiting time between processes of forming gate dielectric and depositing gate electrode is minimized. Preferably, the gate electrode is deposited immediately after form gate dielectric without breaking vacuum.

[0005] Dielectric materials with dielectric constant (k) higher than that of oxynitride are considered as a replacement to pure oxynitride gate dielectric. HfO₂, HfSi_xO_y, HfSi_xO_yN_z are the most promising candidates for the advanced high-k based gate dielectric. (The term "high-k" is used to describe a dielectric material featuring a dielectric constant k which is higher than 3.9 which is the k of SiO₂.) A typical gate dielectric stack with high-k materials is composed of extremely thin silicon oxide, oxynitride, or nitride followed by a high-k material. It was found that the top surface

of a typical high-k material reacts with the gate electrode producing a substantially large fixed electrical charge at the top interface. Electrical properties of the top interface unpredictably vary depending on a chemical state of the top high-k material surface. Subsequently, there is a need of preserving and controlling chemical state of the high-k interface.

[0006] US Patent No. 6,063,670 discloses gate fabrication processes for split-gate transistors. A method for forming an integrated circuit having multiple gate oxide thicknesses is disclosed therein. A circuit (10) is processed up to gate oxide formation. A first gate dielectric (20) is formed. Next, a disposable layer (22) is formed over the first gate dielectric (20). The disposable layer (22) comprises a material that may be removed selectively with respect to silicon and the gate dielectric, such as germanium (Ge). If desired, a second dielectric layer (24) may be formed over the disposable layer (22). A pattern (26) is then formed exposing areas (14) of the circuit where a thinner gate dielectric is desired. The second dielectric layer (24), if it is present, and the disposable layer (22) are removed from the exposed areas. The pattern (26) is then removed. Following pre-gate cleaning, the second gate dielectric (30) is formed. The remaining portions of the disposable layer (22) may be removed either prior to, during, or after the second gate dielectric formation (30).

[0007] US Patent No. 6,140,185 ("Kimura") discloses method of manufacturing semiconductor device. A first gate oxide film is formed on a surface of a silicon substrate. A first polycrystalline silicon film is formed on the first gate oxide film, and patterned so that its side surface is tapered. Silicon oxide film exposed through the first polycrystalline silicon is removed, and a second silicon oxide film having film

thickness different from that of the first silicon oxide film is formed by thermal oxidation. Thus, dual gate oxide is manufactured.

[0008] In FIGs. 14-17, Kimura shows forming a first gate oxide film 1a having a first portion on one side of a field oxide 2 and a second portion on an opposite side of the field oxide. The first portion of the first gate oxide is masked with photoresist (PR) 105a. Wet etching removes the second portion of first gate oxide. Then the photoresist is stripped, and thermal oxidation is performed again. This forms a new, second gate oxide in the second portion, and increases the thickness of the remaining first portion of the first gate oxide. Kimura recognizes that photoresist in contact with the first gate oxide is not desirable, since it contains impurities. Kimura also recognizes that precleaning prior to growing the second gate oxide will also undesirably etch the first gate oxide.

[0009] In FIGs. 18-23, Kimura shows forming a first gate oxide film 1a having a first portion on one side of a field oxide 2 and a second portion on an opposite side of the field oxide. A first polycrystalline silicon film 204a doped with an impurity is formed on the entire surface, as a protective film for the first gate oxide film 1a. The first portion of the first gate oxide is masked with photoresist (PR) 105a. Then, the polysilicon over the second portion of the gate oxide is etched away. Then, the photoresist is stripped, and thermal oxidation is performed again. This forms a new, second gate oxide in the second portion, and forms an oxide coating 6 on the polysilicon over the first portion of the first gate oxide. In this embodiment, the entrance of Na impurities from the photoresist into the first gate oxide is prevented. Therefore, the first gate

oxide film 1a is prevented from being rendered conductive, and variation of the threshold voltage of the MOS transistor is prevented.

[0010] In FIGs. 1-9, Kimura shows forming a first gate oxide film 1a having a first portion on one side of a field oxide 2 and a second portion on an opposite side of the field oxide. A first polycrystalline silicon film 4a doped with an impurity is formed on the entire surface, as a protective film for the first gate oxide film 1a. The first portion of the first gate oxide is masked with photoresist (PR) 5a. Then, the polysilicon over the second portion of the gate oxide is etched away. Then, the photoresist is stripped, and the first polycrystalline silicon film 4a is patterned and inclined to have an angle (tapered shape). Thereafter, the exposed second portion of the first gate oxide film is removed, and thermal oxidation is performed again. This forms a new, second gate oxide 1b in the second portion, and forms an oxide coating 6 on the polysilicon over the first portion of the first gate oxide. Condition of thermal oxidation is set such that the film thickness of the second gate oxide film 1b differs from the film thickness of the first gate oxide film 1a. Thus, dual gate oxide is formed.

[0011] FIGs. 1A-1C illustrate an exemplary prior art technique for forming multiple gate dielectrics (e.g., oxides) on a semiconductor substrate 102. A sequence of steps and structures resulting therefrom are illustrated. For purposes of this discussion, the substrate 102 has a top (as viewed) surface upon which semiconductor devices will be formed, and has two distinct areas (regions) - a left-hand (as viewed) area 102a and a right-hand (as viewed) area 102b. There can be many distinct areas on the semiconductor substrate. The semiconductor substrate 102 is suitably a semiconductor wafer.

- [0012] First, the entire (both left- and right-hand areas) surface of the substrate 102 is prepared/ precleaned, such as with ammonia hydroxide/hydrogen peroxide water mixture (APM, an example of which is "RCA"). Then, a thick dielectric (e.g., thick oxide) 104 is grown or deposited on the entire surface of the substrate 102. The thick dielectric 104 is suitably silicon dioxide (SiO₂) or Silicon Oxynitride (SiON), and suitably has a thickness of approximately 2.0 - 5.5 nm (nanometers) = 20 - 55 Angstroms. The thick dielectric 104 may be grown by thermal oxidation, or it may be deposited by Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD), Atomic Layer Deposition (ALD), or the like.
- [0013] Then, photoresist (PR) 106 is applied and patterned, forming a soft mask for further processing steps, so that a first portion (left-hand side, as viewed) of the thick dielectric 104 is covered with photoresist 106 and a second portion (right-hand side, as viewed) of the thick dielectric 104 is exposed - i.e., it is not covered with photoresist 106. The resulting structure is shown in the cross-sectional view of FIG. 1A.
- [0014] Next, the thick dielectric 104 is etched away in the exposed (not covered by photoresist) areas (portions), such as with hydrofluoric acid (HF) leaving the right-hand surface area of the substrate 102 exposed. And, the photoresist (soft mask) 106 is removed (stripped).
- [0015] Then, the substrate is cleaned, again suitably using an RCA wet clean. The cleaning agent should not contain hydrofluoric acid (HF), because this would etch the desired remaining thick dielectric 104. And, a chemical oxide (chemical ox) 108 forms on the exposed (right-hand) area of the substrate 102. The chemical oxide 108 typically has a thickness of approximately 7 - 12 Angstroms. The resulting structure is shown in the cross-sectional view of FIG. 1B.

[0016] Next, a thin dielectric (e.g., thin oxide) 112 is grown or deposited over the entire surface of the substrate - i.e., over the exposed surface of the thick dielectric 104 and over the exposed surface of the chemical oxide 108. This can be done in the presence of a nitrogen plasma (N PLASMA) 110, so that the dielectric is silicon oxynitride (SiON). The thin dielectric (oxide) 112 suitably has a thickness of approximately 10 - 25 Angstroms. The thin dielectric 112 may be grown by a thermal process, or it may be deposited by a CVD or PVD process.

[0017] The resulting structure is shown in the cross-sectional view of FIG. 1C. In the resulting structure, the left-hand side 102a of the substrate 102 has thick dielectric (104 + 112), and the right-hand side 102b of the substrate 102 has thin dielectric (108 + 112).

[0018] The process described hereinabove can be repeated, multiple times, to achieve more than 2 different oxide thicknesses.

[0019] A number of disadvantages and problems are associated with the prior art process described hereinabove.

- the process sequence must be thicker films (e.g., 104) first, then thinner films (e.g., 112);
- the thick dielectric is exposed to the preclean for the thin dielectric;
- the thick dielectric is exposed to thin gate dielectric growth or deposition process, and

therefore:

- the tolerance on the thick oxide is degraded (exposed to multiple process); and
- final dielectric properties of thick and thin dielectrics are coupled to each other.
- the thin dielectric area will have chemical oxide prior to growth, and HF cannot be used;
- this sequence is not compatible with high-k integration. (If the high-k is deposited first, it will be exposed to the subsequent oxidation and may degrade as well as contaminate the tool. If the high-k is deposited second, it will be deposited in both areas.)

SUMMARY OF THE INVENTION

- [0020] An object of the invention is to provide an improved technique for forming gate oxides (gate dielectrics) having multiple (i.e., different) thickness (and, optionally, different composition) on the same semiconductor substrate, without being constrained to first form thicker films, and while preserving the quality of the top gate dielectric surface.
- [0021] According to the invention, a method of forming different gate oxides on a semiconductor substrate comprises forming a first gate oxide on the top surface of the substrate; depositing a first layer of polysilicon over the first gate oxide; forming a hard mask on top of the first layer of polysilicon; forming a soft mask covering the first gate oxide, first layer of polysilicon and hard mask in the first area of the substrate; removing the hard mask, the first layer of polysilicon and the first gate oxide in the second area of the substrate, leaving the second area exposed; stripping the soft mask; cleaning the exposed second area of the substrate; growing a second gate oxide on the top surface of the substrate in the second area; and removing the hard mask.
- [0022] According to the invention, a method of forming gate oxides on a semiconductor substrate comprises forming a first gate oxide on the top surface of the substrate; protecting the first gate oxide from damage during subsequent processing steps by forming a sacrificial hard mask over a selected area of the first gate oxide; and then forming a second gate oxide.
- [0023] According to the invention, a method of forming at least two different gate dielectrics on a substrate comprises forming a first gate dielectric on a surface of the substrate; forming a first gate electrode on the first gate dielectric; forming a sacrificial hard

mask on the first gate electrode in the first areas of the substrate; removing the first gate electrode and the first gate dielectric in the second areas of the substrate; cleaning and oxidizing the second areas of the substrate to form a second gate dielectric; removing the sacrificial mask selective to the second gate dielectric; and depositing a second gate electrode electrically connected to the first gate electrode.

[0024] According to the invention, an electronic system incorporates at least one IC chip formed by forming a first gate oxide on the top surface of a semiconductor substrate; protecting the first gate oxide from damage during subsequent processing steps by forming a sacrificial hard mask over a selected area of the first gate oxide; and then forming a second gate oxide on the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0025] The structure, operation, and advantages of the present invention will become further apparent upon consideration of the following description taken in conjunction with the accompanying figures (FIGs.). The figures are intended to be illustrative, not limiting. Certain elements in some of the figures may be omitted, or illustrated not-to-scale, for illustrative clarity. The cross-sectional views may be in the form of "slices", or "near-sighted" cross-sectional views, omitting certain background lines which would otherwise be visible in a "true" cross-sectional view, for illustrative clarity.
- [0026] FIGs. 1A-1C are cross-sectional views illustrating a sequence of steps in a process for forming multiple gate dielectrics on a semiconductor substrate, according to the prior art.
- [0027] FIGs. 2A-2E are cross-sectional views illustrating a sequence of steps in a process for forming multiple gate dielectrics on a semiconductor substrate, according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0028] In the description that follows, numerous details are set forth in order to provide a thorough understanding of the present invention. It will be appreciated by those skilled in the art that variations of these specific details are possible while still achieving the results of the present invention. Well-known processing steps are generally not described in detail in order to avoid unnecessarily obfuscating the description of the present invention.

[0029] In the description that follows, exemplary dimensions are presented for an illustrative embodiment of the invention. The dimensions should not be interpreted as limiting. They are included to provide a sense of proportion. Generally speaking, it is the relationship between various elements, where they are located, their contrasting compositions, and sometimes their relative sizes that is of significance.

[0030] FIGs. 2A-2E illustrate an embodiment of a technique for forming multiple gate dielectrics on a semiconductor substrate 202 (compare 102). A sequence of steps and structures resulting therefrom are illustrated.

[0031] For purposes of this discussion, the substrate 202 has a top (as viewed) surface upon which semiconductor devices will be formed, and has two distinct areas - a first (left-hand, as viewed) area 202a and a second (right-hand, as viewed) area 202b which is distinct from the first area. There can be many distinct areas on the semiconductor substrate. The semiconductor substrate 202 is suitably a semiconductor wafer.

[0032] First, the entire (both left- and right-hand portions) surface of the substrate 202 is pre-cleaned, such as with RCA. Then, a first gate oxide 204 (DIELECTRIC-1, compare 104) is formed (grown or deposited) on the entire surface of the substrate 102. The first gate oxide 204 is suitably silicon dioxide (SiO₂), silicon oxynitride (SiON), silicon nitride (SiN) or high-k, and suitably has a thickness of approximately 5 - 25 Angstroms, such as 20 - 25 Angstroms. The first gate oxide 204 may be grown or deposited using known processes.

[0033] Then, a thin layer of polysilicon (also "poly-Si", or simply "poly") 206 which will function as a gate electrode is deposited on the entire exposed surface of first gate oxide 204, using known processes. The layer of polysilicon 206 suitably has a thickness of approximately 2-50 nm (20 - 500 Angstroms).

[0034] Then, a hard mask 208 is deposited on the entire exposed surface of the layer of polysilicon 206, using known processes. The hard mask 208 is suitably germanium (Ge), silicon germanium (SiGe), amorphous carbon, SiO₂, Si₃N₄, or other materials that are easy to remove from a silicon wafer without leaving a residue. The hard mask 208 suitably has an initial thickness of approximately 30-50 nm (300-500 Angstroms). As will become evident, the hard mask is sacrificial in that after it serves the purpose of protecting the first gate oxide 204 from subsequent process steps, it can be removed, notably without damaging the subsequently formed second gate oxide (212, described hereinbelow).

- [0035] Then, photoresist (PR) 210 (compare 106) is applied and patterned, forming a soft mask for further processing steps, so that a first portion (left-hand side, as viewed) of the stack of gate oxide 204 / poly-Si 206 / hard mask 208 is covered with photoresist 210 and a second portion (right-hand side, as viewed) is exposed - i.e., not covered with photoresist. The photoresist serves as a soft mask. The soft mask 210 covers the first gate dielectric, first layer of polysilicon and hard mask in the first area 202a of the substrate - i.e., a first gate oxide stack. The soft mask 210 leaves exposed the first gate dielectric, first layer of polysilicon and hard mask in the second area 202b of the substrate - i.e., a second gate oxide stack.
- [0036] Then, the exposed areas of the hard mask 208 / poly-Si 206 and DIELECTRIC-1 206 are removed, using standard etching processes such as reactive ion etching (RIE) or wet etching, down to the surface of the substrate 202. The resulting structure is shown in the cross-sectional view of FIG. 2A.
- [0037] Next, the photoresist 210 is stripped using standard techniques (e.g., mixture of H₂SO₄ and H₂O₂). During photoresist strip, the hard mask (Ge) 208' may be partially etched, for example having a thickness of approximately up to 50% less than shown in FIG. 2A. Therefore, the initial thickness of the hard mask 208 must be chosen to ensure that after photoresist strip, a sufficient thickness of hard mask remains. For example, a sufficient remaining thickness would be approximately at least 1.5 nm (15 Angstroms) left after PR strip. The thickness of the hard mask material that remains in place on the substrate after stripping the substrate should be sufficient to be consumed during the second oxidation process (described below) and not allow any

poly-Si to be oxidized. Thus, the thickness depends on the second oxide thickness and process conditions.

[0038] The resulting structure is shown in the cross-sectional view of FIG. 2B wherein the slightly etched hard mask 208' is shown with a primed (') number indicating that it has been altered (in this case, thinned) between the views of FIGs. 2A and 2B.

[0039] Next, standard surface preparations are made for forming a second dielectric (DIELECTRIC 2). As is evident, the top of gate oxide 204 is protected from damage during this pre-clean step by the overlying layers of poly-Si 206 and hard mask 208.

[0040] Next, a second dielectric (DIELECTRIC-2) 212 is grown. Gate oxide 204 is protected from damage during this step by the overlying layers of poly-Si 206 and hard mask 208. The second dielectric (gate oxide) 210 is suitably silicon dioxide (SiO₂), silicon oxynitride (SiON), silicon nitride (SiN) or high-k material, grown by:

- rapid thermal oxidation (RTO) in NO, N₂O, NH₃, O₂ (500-1100 degrees C); or
- plasma nitridation treatment on base oxide (25 - 800 degrees C);
- plasma oxidation; UV oxidation; atomic layer deposition.

[0041] The second dielectric 212 has an exemplary thickness of approximately 35-40 Angstroms.

[0042] During this step, the hard mask (Ge) 208' on top of the DIELECTRIC-1 areas will be oxidized, and a layer of germanium oxide (GeO₂) 214 will be formed. The resulting

structure is shown in the cross-sectional view of FIG. 2C wherein the slightly oxidized hard mask 208" is shown with a double-primed (") number indicating that it has been altered (in this case, oxidized) between the views of FIGs. 2B and 2C.

[0043] It should be noted that the thin poly-Si 206 is also protected from oxidation from the overlying hard mask 208' (208"). It should also be noted that the thickness of the hard mask 208 should be chosen such that it is not entirely consumed by the oxidation process.

[0044] Next, the mask oxide (GeO₂) 214 is removed using an etch that will remove the GeO₂ without affecting (selective to) the second dielectric 212. For example, remove GeO₂ with a water rinse since it is water soluble, which will not etch the second dielectric 212. Then, the remaining hard mask (Ge) material 208" is removed, selective to SiO₂ and polysilicon. For example, remove the Ge with an H₂O₂ rinse. The resulting structure is shown in the cross-sectional view of FIG. 2D

[0045] Herein it should be noted that the thin polysilicon 206 has remained in place on top of the first gate oxide 204 throughout the process sequence. Since it is never removed, and remains part of the final structure, the thin polysilicon 206 serves to preserve the high quality of the first gate oxide 204. This enables, among other things, the use of high-k material for the first gate oxide 204.

[0046] Next, gate polysilicon 216 (for a second gate electrode) is deposited on top of the entire wafer 202, including the first gate oxide 204 which is already covered by a thin

protective layer of polysilicon 206, and including on top of the second dielectric 212. The gate polysilicon 216 may be deposited by a standard process such as low pressure chemical vapor deposition (LPCVD; furnace) or room temperature chemical vapor deposition (RTCVD; single wafer reactor) with SiH₄ or other silicon precursor. The temperature for gate polysilicon 216 deposition is suitably approximately 500 - 800 degrees C, preferably approximately 550 - 650 degrees C, and the resulting thickness of the polysilicon 216 is suitably approximately 500 - 2000 Angstroms. Note that because the previously deposited polysilicon layer 206 is thin (typically < 50 Angstroms), the planarity of the gate poly stack is maintained, which is beneficial for subsequent process steps such as gate poly lithography (not shown). The resulting structure is shown in the cross-sectional view of FIG. 2E. In the resulting structure, the left-hand side 202a of the substrate 202 has thin gate oxide (204) , and the right-hand side 202b of the substrate 202 has thick gate dielectric (212).

[0047] Finally, remaining integrated circuit (IC) process steps may proceed in a standard process flow. The process can be performed multiple times to produce more than 2 gate oxide thicknesses. For example, the process described above can be repeated to produce a third gate oxide in a third area of the semiconductor substrate, said third gate oxide having a thickness which is different than either of the first and second gate oxides.

[0048] The technique described hereinabove is useful for forming gate oxides of multiple thicknesses, as well as for allowing a thin oxide to be formed before a thicker oxide, and for using high-k materials in gate oxides.

[0049] Regarding thicknesses, it is generally contemplated that the thinnest useful gate oxide thickness is approximately 10 Angstroms, and the thickest useful gate oxide thickness is approximately 55 Angstroms. Examples of multiple gate oxide thicknesses would be 12 and 15 Angstroms, or 15 and 30 Angstroms. In any case, the second gate oxide may have a thickness that is significantly different, from a viewpoint of electrical performance (as described above) than that of the first gate oxide, or it may be compositionally different.

[0050] The advantages and benefits of the technique described hereinabove include:

- "Dielectric-1" (gate oxide) 204 is always covered, therefore:
- a high-k dielectric can be used, without danger of cross-contamination
- the quality of this dielectric is maintained by avoiding exposure to uncontrolled atmosphere and subsequent process steps. It is known that for high-k, this top interface is the key for achieving desired V_t (threshold voltage) control.
- decoupling of multiple gate dielectrics on a single chip;
- ability to use HF-based precleans for all gate oxides;
- wide gate oxide thickness range for different devices;
- reduction of substrate Si loss, which may be important for thin silicon-on-insulator (SOI) and strained Si substrates

[0051] The first gate oxide 204 can be a high-k material, such as HfO_2 , HfSi_xO_y , $\text{HfSi}_x\text{O}_y\text{N}_z$, etc. As mentioned, one of the advantages of the present invention is that a high-k material (e.g., for 204), being covered with polysilicon (e.g., 206), can be used in a process for forming multiple gate oxide thicknesses, without danger of cross-

contamination. In contrast with a process wherein a high-k first dielectric were not covered by polysilicon, it can be noted that:

when the high-k is covered with polysilicon

- the poly protects the high-k / poly interface; and
- the poly prevents the high-k from contaminating the process tool or other parts of the same wafer.

when the high-k is not covered with polysilicon

- during processing, such as wet process or furnace deposition of polysilicon, the high-K is exposed and can result in contamination of the process tool or other parts of the same wafer.
- the exposed surface of high-k may degrade.

[0052] In the method described hereinabove, the thin oxide is formed first and then capped with poly. The poly may or may not contain Ge or carbon (C) to control gate activation and boron (B) penetration. The poly is then removed over areas (e.g., 202b) where thick oxide is to be grown. With this method or repetition of this method, multiple oxides can be fabricated with minimal interference with each other.

[0053] The benefits of the present invention include:

- the thinnest oxide can be grown independently from other oxides;
- the surface for the thin oxide growth is the most pristine surface (as opposed to having DG oxide strip and PR removal etch chemical oxide);
- option of using HF-base precleans for gate oxides;
- thin oxide capping enable easier integration of high-k materials; and
- silicon consumption is minimized in thin gate region because addition oxidation strip does not cause additional silicon consumption in the thin oxide area (important for

strained silicon – loss of strained silicon layer should be minimized as much as possible).

[0054] The present invention may be contrasted, for example, with Kimura. The hard mask used in the present invention enables processing the entire structure in a much easier and efficient way in that it is possible to keep the poly height constant for all of the oxide thicknesses. Furthermore, since Kimura uses a non-disposable poly layer as a hard mask, that poly will be exposed to the thermal cycle of the second gate oxide. This may cause undesired grain growth. For the present invention, only the thin poly is exposed to the second thermal cycle - the disposable Ge will be removed anyway and fresh poly will be deposited. Furthermore, Kimura's technique required an additional lithography step formed only on the right side (see Figure 6). Since the poly in the present invention is relatively thin, an additional lithography step is not necessarily required (see Figure 2E.). Thus, the inventive technique is not subject to the tolerance associated with two lithography steps. Furthermore, the present invention does not require etching the poly back as in Figure 6 of Kimura, rather any mask on the poly surface is removed prior to the second oxide deposition and thus there is no reason to etch back. This is a much simpler method. Additionally, for the purpose of incorporating more than two oxides, the thick barrier of the present invention is a better stopping layer than the thin barrier in Kimura's technique.

[0055] The soft mask resist process (e.g., Kimura) has the drawback that the soft mask must be removed prior to gate dielectric process. Once it is removed, it cannot block the gate dielectric process from going onto the whole wafer. The result is that the later gate dielectric process will affect previously grown/deposited gate dielectric areas.

- [0056] In contrast thereto, by using a hard mask which can withstand and block gate dielectric process, the present invention enables selectively placing gate dielectric in the desired areas. This effectively decouples the different gate dielectric processes and areas from each other. This allows for independent optimization of the multiple on-chip dielectrics.
- [0057] A variety of integrated circuit (IC) chips having circuits formed utilizing the techniques described hereinabove, and such chips can be integrated with other electronic components and subsystems to realize a subsystem or a system having electrical functionality such as, but not limited to memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.
- [0058] The invention has been illustrated and described in a manner that should be considered as exemplary rather than restrictive in character - it being understood that all changes and modifications that come within the scope of the invention as set forth in the claims